WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor integrated circuit, comprising:

providing a dielectric portion;

etching the dielectric portion to produce a feature;

during said etching step, providing on the feature a liner material to produce a lined feature; and

depositing a conductive material on the lined feature.

2. The method of Claim 1, wherein said etching step includes reactive ion etching.

3. The method of Claim 1, wherein said etching step includes reactive ion etching, wherein said liner is a metallic liner, and wherein said liner providing step includes redepositing sputter products from a metal hardmask during said reactive ion etching step.

4. The method of Claim 3, wherein said reactive ion etching step includes using a fluorocarbon gas.

5. The method of Claim 4, wherein the fluorocarbon gas is CF_4.

6. The method of Claim 3, wherein the metal hardmask is TaN.

7. The method of Claim 6, wherein said reactive ion etching step includes using a fluorocarbon gas.

8. The method of Claim 1, wherein the dielectric portion includes a low-k dielectric.

9. The method of Claim 1, wherein the dielectric portion includes an organic dielectric.

10. The method of Claim 1, including providing a seed layer on the liner material before said depositing step.

11. The method of Claim 1, wherein said conductive material is copper.

12. The method of Claim 1, wherein the feature is one of a trench and a via hole.

13. The method of Claim 1, wherein said etching step includes reactive ion etching, said reactive ion etching step including using a TEL SCCM etch tool.

14. The method of Claim 1, wherein said etching step includes etching through a dielectric hardmask of the dielectric portion, said step of etching through the dielectric hardmask including using pressure in a range of 30 mT-100mT, using total RF power above approximately 800 watts, using an Ar flow rate in a range of 350-700 sccm, using an O_2 flow rate in a range of 10-30 sccm, and using one of a CF_4 flow rate in a range of 10-45 sccm and a CHF_3 flow rate in a range of 10-45 sccm.

15. The method of Claim 14, wherein said etching step includes etching an organic dielectric of the dielectric portion, said step of etching the organic dielectric including using an etch gas that is a mixture of N_2 at a flow rate of approximately 300 sccm and H_2 at a flow rate of approximately 300 sccm, and using a total RF power of approximately 3000 watts.

16. A semiconductor integrated circuit fabricated according to the method of Claim 1.

17. A method of fabricating a semiconductor integrated circuit, comprising:

providing a dielectric portion;

in an etch chamber, etching the dielectric portion to produce a feature;

in said etch chamber, providing on the feature a liner material to produce a lined feature; and

depositing a conductive material on the lined feature.

18. The method of Claim 17, wherein said etching step includes reactive ion etching, wherein said liner is a metallic liner, and wherein said liner providing step includes redepositing sputter products from a metal hardmask during said reactive ion etching step.

19. The method of Claim 17, wherein said etching step includes etching through a dielectric hardmask of the dielectric portion, said step of etching through the dielectric hardmask including using pressure in a range of 30 mT-100mT, using total RF power above approximately 800 watts, using an Ar flow rate in a range of 350-700 sccm, using an O_2 flow rate in a range of 10-30 sccm, and using one of a CF_4 flow rate in a range of 10-45 sccm and a CHF_3 flow rate in a range of 10-45 sccm.

20. The method of Claim 19, wherein said etching step includes etching an organic dielectric of the dielectric portion, said step of etching the organic dielectric including using an etch gas that is a mixture of N_2 at a flow rate of approximately 300 sccm and H_2 at a flow rate of approximately 300 sccm, and using a total RF power of approximately 3000 watts.

21. A semiconductor integrated circuit fabricated according to the method of Claim 17.

22. A method of fabricating a semiconductor integrated circuit, comprising:

providing a low-k dielectric portion;

reactive ion etching the low-k dielectric portion to produce a feature;

during said reactive ion etching step, providing on the feature a metallic liner material to produce a lined feature; and

depositing copper on the lined feature.

23. A semiconductor integrated circuit fabricated according to the method of Claim 22.

24. A method of fabricating a semiconductor integrated circuit, comprising:

providing a low-k dielectric portion;

in an etch chamber, reactive ion etching the low-k dielectric portion to produce a feature;

in said etch chamber, providing on the feature a metallic liner material to produce a lined feature; and

depositing copper on the lined feature.

25. A semiconductor integrated circuit fabricating according to the method of Claim 24.